Integrated Video input processor and Teletext decoder (IVT1.8*)

SAA5281

FEATURES

- Complete Teletext and VPS decoding in a single package
- Built-in 8K × 8 memory for up to 8 page storage
- Enhanced mode allows 7 Fastext pages and 8 pages of TOP to be captured
- Ability to request only subtitle pages
- Acquisition and decoding of VPS data
- Data valid output available to indicate reception of error-free VPS or packet 8/30/2 data
- Software and hardware compatible with SAA5246 and SAA5248
- Meshing display within boxes
- Separate data checking algorithms and pointers for each acquisition channel
- 24 : 18 Hamming checker
- Automatic packet 26 extension character processing
- Indication of Line 23 for external use
- 13.5 MHz clock output to drive external microcontroller
- Detection of Spanish transmissions to disable flicker-stopper
- Compatible with Philips' one-chip TV IC (TDA836X) for scan-locking applications.

DESCRIPTION

The IVT1.8* is a single-chip Teletext decoder IC for decoding 625-line based World System Teletext transmissions. The device is based on IVT1.0VPS and has reception facilities for the 5 MHz biphase VPS signal. It is intended for use in video recorders, in particular to implement the VPT facility (VCR programming via Teletext). With suitable software both VPT standards (EBU PDC System A and System B) can be accommodated to allow operation from any European VPT transmission. Automatic processing of packet 26 transmissions is also possible. No external memory is required as an 8K × 8 DRAM is included on-chip for up to 8 page storage. An enhanced mode allows 7 Fastext pages to be stored, with one chapter used to store extension packets.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	75	150	mA
V_{sync}	sync voltage amplitude	0.1	0.3	0.6	V
$V_{vid(p-p)}$	video input voltage amplitude (peak-to-peak value)	0.7	1.0	1.4	V
f_{xtal}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5281P	48	DIP48	plastic	SOT240-1
SAA5281ZP	52	SDIP52	plastic	SOT247-1

BLOCK DIAGRAM

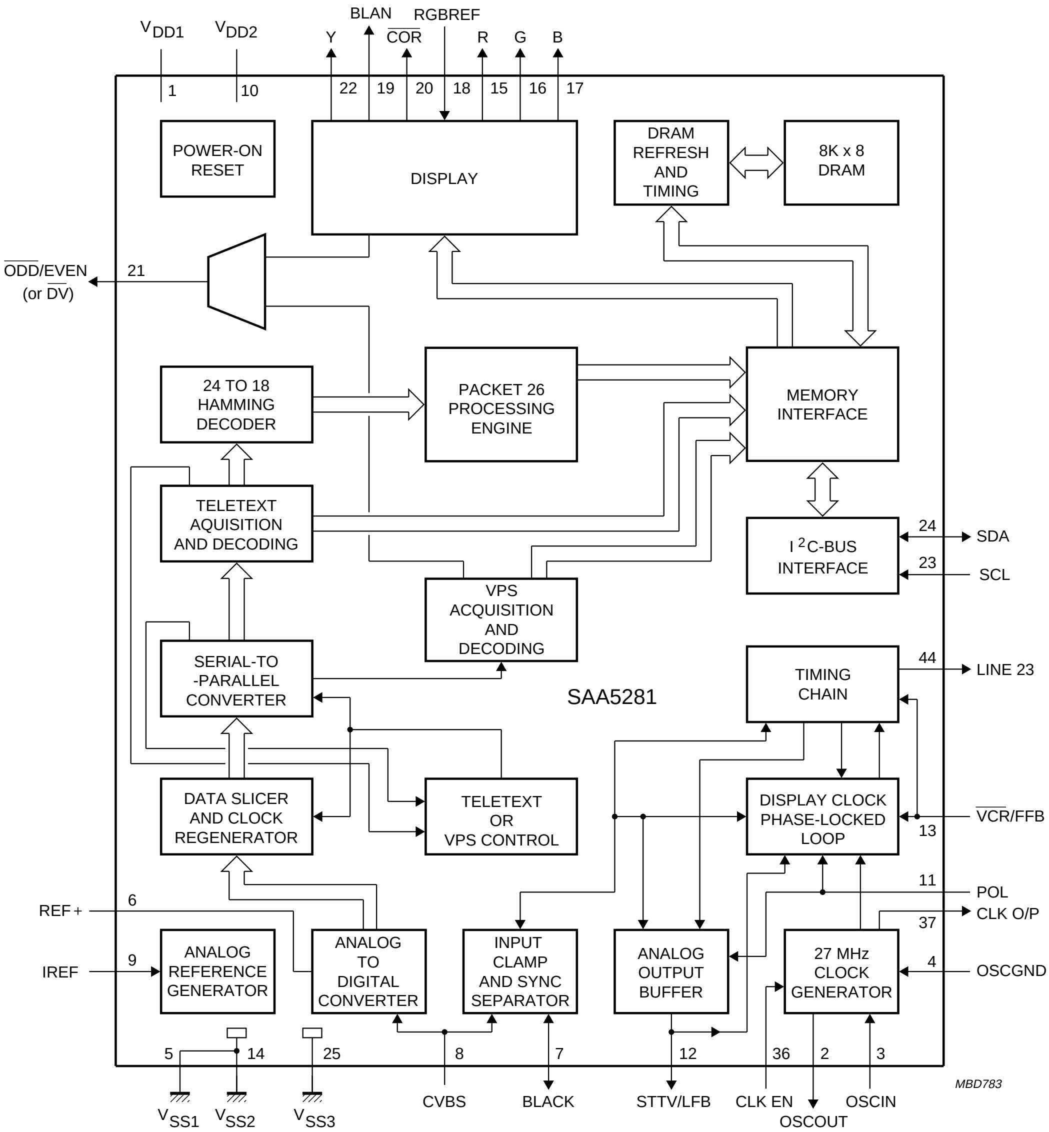


Fig.1 Block diagram; pin numbers for DIP48 (SOT240-1).

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT240-1	SOT247-1	
V_{DD1}	1	52	+5 V supply 1.
OSCOUT	2	1	27 MHz crystal oscillator output.
OSCIN	3	2	27 MHz crystal oscillator input.
OSCGND	4	3	0 V crystal oscillator ground.
V_{SS1}	5	4, 5	0 V ground.
REF+	6	6	Positive reference voltage for ADC. This pin should be connected to ground via a 100 nF capacitor.
BLACK	7	8	Video black level storage input/output. This pin should be connected to ground via a 100 nF capacitor.
CVBS	8	9	Composite video input. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor.
IREF	9	10	Reference current input, connected to ground via a 27 kΩ resistor.
V_{DD2}	10	11	+5 V supply 2.
POL	11	12	STTV/LFB/FFB polarity selection input.
STTV/LFB	12	13	Sync to TV output line flyback input. Function controlled by an internal register bit (scan sync mode).
$\overline{\text{VCR}}$/FFB	13	14	PLL time constant switch/field input. Function controlled by an internal register bit (scan sync mode).
V_{SS2}	14	15	0 V ground; connected to V_{SS1} for normal operation.
R	15	16	Dot rate character output of the RED colour information.
G	16	17	Dot rate character output of the GREEN colour information.
B	17	18	Dot rate character output of the BLUE colour information.
RGBREF	18	19	Input DC voltage to define the output high level on the RGB pins.
BLAN	19	20	Dot rate fast blanking output.
$\overline{\text{COR}}$	20	21	Programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open-drain output.
$\overline{\text{ODD}}$/EVEN (or $\overline{\text{DV}}$)	21	22	In $\overline{\text{ODD}}$/EVEN mode a 25 Hz output synchronized with the CVBS input field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents. In $\overline{\text{DV}}$ mode a VPT data valid signal is used to indicate reception of error-free VPS or 8/30 format 2 data.
Y	22	23	Dot rate character output of teletext foreground colour information. Open-drain output.
SCL	23	24	Serial clock input for I^2C-bus. It can still be driven HIGH during power-down of the device.
SDA	24	25	Serial data port for the I^2C-bus. Open-drain output. It can still be driven HIGH during power-down of the device.
V_{SS3}	25	26	0 V ground.
i.c.	26 to 35, 38 to 43, 45 to 48	27 to 32, 35 to 38, 41 to 46, 48 to 51	Internally connected. Normally open-circuit.

SYMBOL	PIN		DESCRIPTION
	SOT240-1	SOT247-1	
CLK EN	36	39	Clock enable input to enable the clock output (CLP O/P; pin 37). Internal pull-down normally disables clock.
CLK O/P	37	40	13.5 MHz clock output to drive an external microcontroller.
LINE 23	44	47	Output for indication of Line 23 for use with external circuitry.
n.c.	–	7, 33, 34	Not connected. Normally open-circuit.

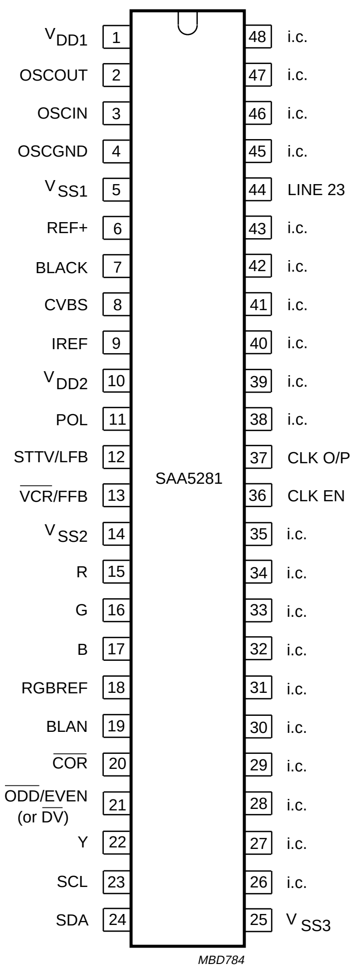


Fig.2 Pin configuration; SOT240-1 (DIP48).

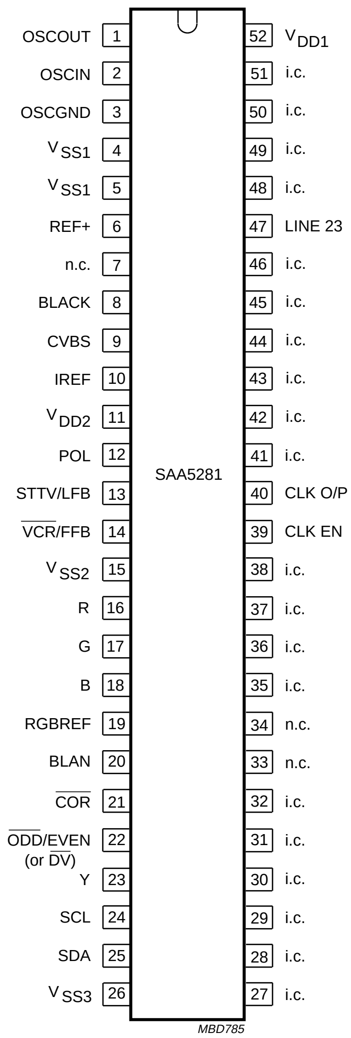


Fig.3 Pin configuration; SOT247-1 (SDIP52).

QUALITY AND RELIABILITY

This device will meet Philips Semiconductors General Quality Specification for Business group *"Consumer Integrated Circuits SNW-FQ-611-Part E"*. The principal requirements are shown in Tables 1 to 4.

Group A

Table 1 Acceptance tests per lot.

TEST	REQUIREMENTS(1)
Mechanical	cumulative target: <100 ppm
Electrical	cumulative target: <100 ppm

Group B

Table 2 Processability tests (by package family).

TEST	REQUIREMENTS(1)
Solderability	<7% LTPD
Mechanical	<15% LTPD
Solder heat resistance	<15% LTPD

Group C

Table 3 Reliability tests (by process family).

TEST	CONDITIONS	REQUIREMENTS(1)
Operational life	168 hours at T_j = 150 °C	<1500 FPM; equivalent to <100 FITS at T_j = 70 °C
Humidity life	temperature, humidity, bias 1000 hours, 85 °C, 85% RH (or equivalent test)	<2000 FPM
Temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	<2000 FPM

Table 4 Reliability tests (by device type).

TEST	CONDITIONS	REQUIREMENTS(1)
ESD and latch-up	ESD Human body model 2000 V, 100 pF, 1.5 kΩ	<15% LTPD
	ESD Machine model 200 V, 200 pF, 0 Ω	<15% LTPD
	latch-up 100 mA, 1.5 × V_{DD} (absolute maximum)	<15% LTPD

Notes to Tables 1 to 4

1. ppm = fraction of defective devices, in parts per million.
   LTPD = Lot Tolerance Percent Defective.
   FPM = fraction of devices failing at test condition, in Failures Per Million.
   FITS = Failures In Time Standard.

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	–0.3	+6.5	V
V_I	input voltage (any input)	–0.3	V_{DD} + 0.5	V
V_O	output voltage (any output)	–0.3	V_{DD} + 0.5	V
I_O	output current (each output)	–	±10	mA
I_{IOK}	DC input or output diode current	–	±20	mA
T_{amb}	operating ambient temperature	–20	+70	°C

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = –20 to +70 °C; pin numbers refer DIP48 package; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DDtot}	total supply current		–	75	150	mA
Inputs						
CVBS						
V_{sync}	sync voltage amplitude		0.1	0.3	0.6	V
$V_{burst(p-p)}$	colour burst amplitude (peak-to-peak value)		0.0	0.3	4.0	V
$t_{d(sync)}$	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		–150	0	+150	ns
$\Delta t_{d(sync)}$	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input voltage amplitude (peak-to-peak value)		0.7	1.0	1.4	V
$V_{dat(text)}$	teletext data voltage amplitude		0.29	0.46	0.71	V
$\Delta f/f$	display PLL capture range		±7	–	–	%
Z_{source}	source impedance		–	–	250	Ω
V_I	input switching voltage level of sync separator		1.7	2.0	2.3	V
Z_I	input impedance		2.5	5.0	–	kΩ
C_I	input capacitance		–	–	10	pF
IREF						
R_{gnd}	resistor to ground		–	27	–	kΩ
V_i	input voltage		–	$0.5V_{DD}$	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
POL						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
LFB						
V_{IL}	LOW level input voltage		–0.3	–	tbf	V
V_{IH}	HIGH level input voltage		tbf	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
I_{Imax}	maximum input current	note 1	–1	–	+1	mA
t_{dLFB}	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
I_{Imax}	maximum input current	note 1	–1	–	+1	mA
RGBREF						
V_{IL}	LOW level input voltage		–0.3	–	V_{DD}	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
SCL						
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
f_{clk}	clock frequency		0	–	100	kHz
t_r	input rise time	between 10% and 90%	–	–	2	µs
t_f	input fall time	between 90% and 10%	–	–	2	µs
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
$V_{osc(p-p)}$	oscillator voltage amplitude (peak-to-peak value)		–	1.0	–	V
G_v	small signal voltage gain		–	1.0	–	
G_m	mutual conductance		5.0	–	–	mS
C_I	input capacitance		–	–	10	pF
C_{fb}	feedback capacitance		–	1	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BLACK						
C_{black}	storage capacitor to ground		–	100	–	nF
V_{black}	black level voltage for nominal sync amplitude		1.8	2.15	2.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
SDA (OPEN-DRAIN INPUT/OUTPUT)						
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	400	pF
t_r	input rise time	between 10% and 90%	–	–	2	µs
t_f	input fall time	between 90% and 10%	–	–	2	µs
t_f	output fall time	between 3 V and 1 V	–	–	200	ns
Outputs						
STTV						
G_{sttv}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS voltage amplitude		0.2	0.3	0.45	V
ΔV_{tcs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
R, G AND B						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA; V_{RGBREF} < V_{DD} – 2 V; note 2	V_{RGBREF} – 0.25	V_{RGBREF}	V_{RGBREF} + 0.5	V
$\|Z_o\|$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10% and 90%	–	–	20	ns
t_f	output fall time	between 90% and 10%	–	–	20	ns
BLAN						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = – 0.2 mA	1.1	–	–	V
		I_{OH} = 0 mA	–	–	2.8	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10% and 90%	–	–	20	ns
t_f	output fall time	between 90% and 10%	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\overline{ODD}$/EVEN OR $\overline{DV}$						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	between 0.6 V and 2.2 V	–	–	50	ns
t_f	output fall time	between 0.6 V and 2.2 V	–	–	50	ns
$\overline{COR}$ AND Y (OPEN-DRAIN OUTPUTS)						
V_{OH}	HIGH level pull-up output voltage		–	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.4	V
		I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} – 0.5 V and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	–10	–	+10	μA
t_{skew}	skew delay between display outputs R, G, B, $\overline{COR}$, Y and BLAN		–	–	20	ns
I²C-bus timing (see Fig.4)						
t_{LOW}	SCL clock LOW time		4.0	–	–	μs
t_{HIGH}	SCL clock HIGH time		4.0	–	–	μs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4.0	–	–	μs
t_{BUF}	START set-up time following a STOP		4.0	–	–	μs
$t_{HD;STA}$	START hold time		4.0	–	–	μs
$t_{SU;STA}$	START set-up time following a clock LOW-to-HIGH transition		4.0	–	–	μs

Notes

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ±1 mA.
2. Voltage level V_{OH} for R, G and B outputs is taken to be the mean value during the output HIGH time. If higher R, G and B voltage V_{OH} levels are required RGBREF voltage level may be raised and a pull-up resistor used at each of these pins provided current specification (I_{OL}) is not exceeded.

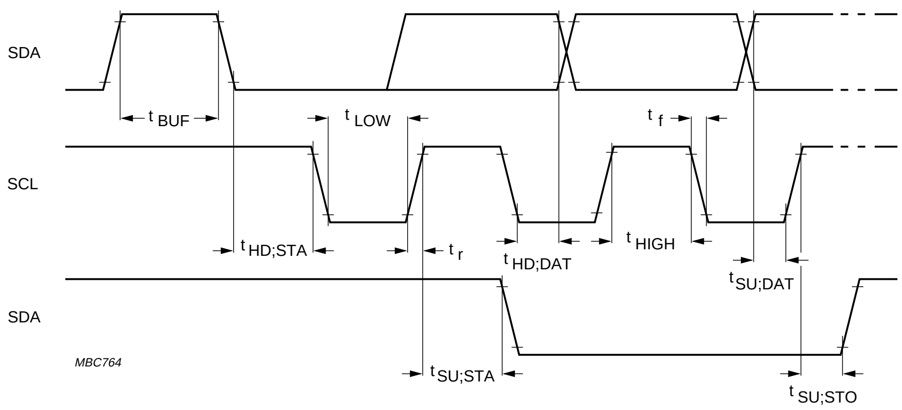
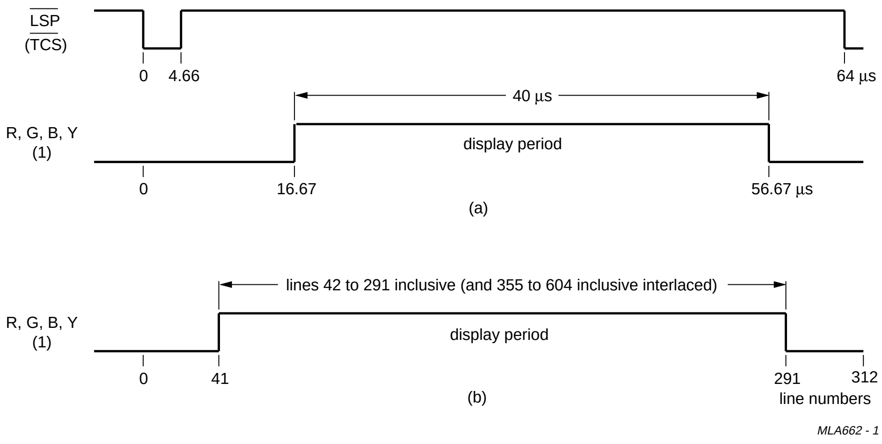


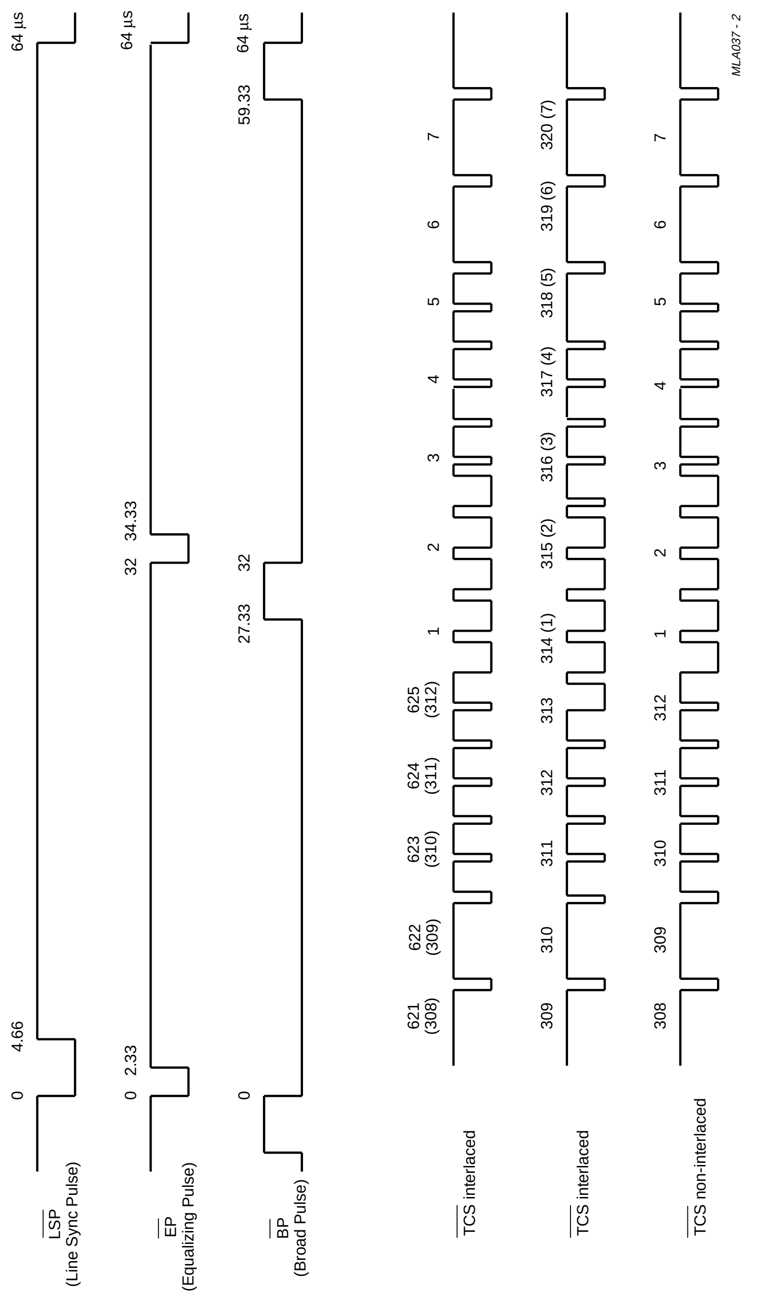
Fig.4 I^{2}C-bus timing.

TIMING CHAIN



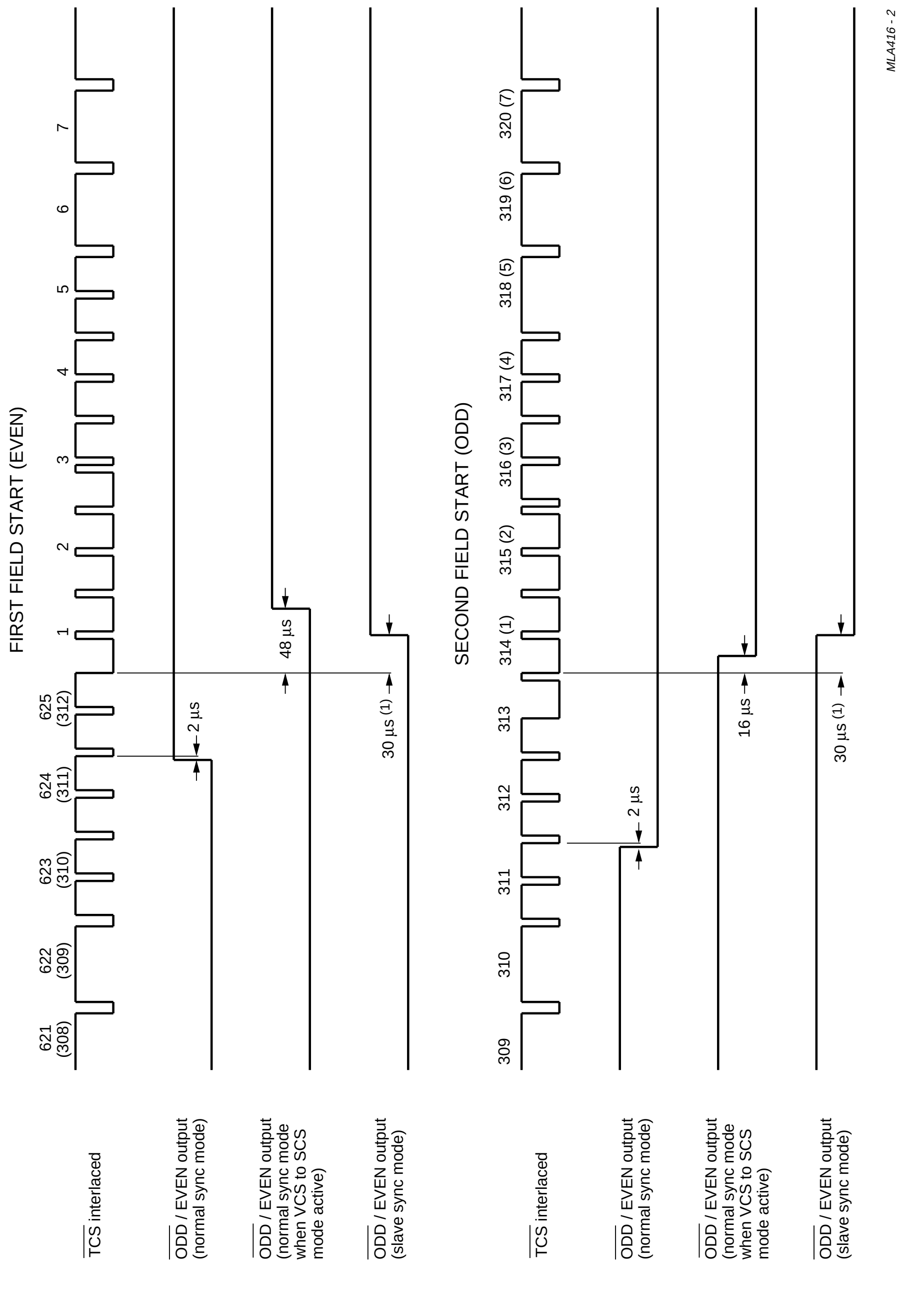
(1) Also BLAN in character and box blanking.

Fig.5 Display output timing (a) line rate (b) field rate.



$\overline{LSP}$, $\overline{EP}$ and $\overline{BP}$ are combined to give $\overline{TCS}$ as shown. All timings are measured from falling edge of LSP.
Line numbers placed in the middle of the line.
Equivalent count numbers in brackets.

Fig.6 Composite sync waveforms.



Line numbers placed in the middle of the line.
Equivalent count numbers in brackets.
(1) Or 62 µs if Register 1 D2.D1.D0 equals 1 1 1.

Fig.7 ODD/EVEN timing.

ON-CHIP MEMORY

Page memory organization

The organization of the page memory is illustrated by Fig.8. The IVT1.8* provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.

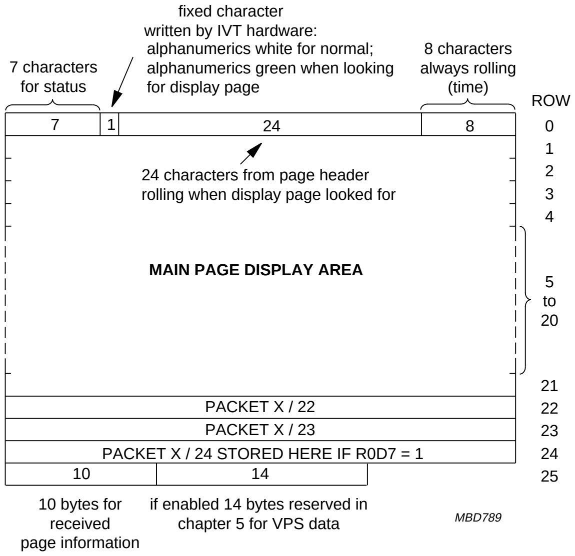


Fig.8 Basic page memory organization.

REMARK TO FIG.8

Row 0

Row 0 is for the page header. The first seven characters (0 to 6) are free for status messages. Character 8 is an alphanumeric white or green control character, written automatically by IVT1.8* to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page as shown in Table 5. The remaining 14 bytes are free for use by the microcomputer.

Table 5 Row 25 received control data format.

ROW 25										
D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Table 6 Page number and sub-code for Table 5.

BIT NAME	DESCRIPTION
Page number	
MAG	magazine
PU	page units
PT	page tens
PBLF	page being looked for
$\overline{\text{FOUND}}$	LOW for page has been found
HAM.ER	Hamming error in corresponding byte
Page sub-code	
MU	minutes units
MT	minutes tens
HU	hours units
HT	hours tens
C4 to C14	transmitted control bits

Extension packet memory organization

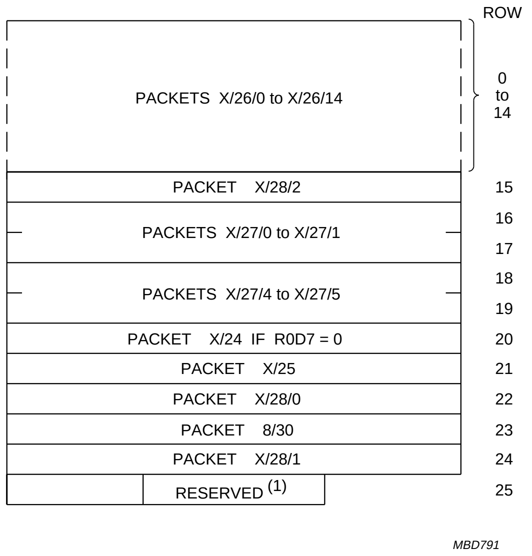
When in normal extension packet enabled mode the rows of information are organized as illustrated in Fig.9.

Row 23 of the extension page, as shown in Fig.9, contains packet 8/30. Packet 8/30 is mapped into the IVT1.8* memory as follows:

8/30/0 and 8/30/1 to Chapter 4 Row 23

8/30/2 and 8/30/3 to Chapter 5 Row 23

8/30/4 to 8/30/15 to Chapter 6 Row 23.



(1) Row 25 reserved for VPS data in Chapter 5.

Fig.9 Organization of the extension memory.

ENHANCED MODE

In enhanced mode, the number of extension packets captured is reduced to the minimum required for FASTEXT operation. The first seven chapters can then be used for storage, using the system of pointers. The arrangement of extension packets is shown in Fig.10.

When in enhanced mode and extension packets are disabled, normal 8-page mode is in operation, but the X/26 engine is enabled (unlike normal 8-page mode).

	ROW
CHAPTER 0 PACKET 24	0
CHAPTER 0 PACKETS 27 / 0	1
CHAPTER 1 PACKET 24	2
CHAPTER 1 PACKETS 27 / 0	3
CHAPTER 2 PACKET 24	4
CHAPTER 2 PACKETS 27 / 0	5
CHAPTER 3 PACKET 24	6
CHAPTER 3 PACKETS 27 / 0	7
CHAPTER 4 PACKET 24	8
CHAPTER 4 PACKETS 27 / 0	9
CHAPTER 5 PACKET 24	10
CHAPTER 5 PACKETS 27 / 0	11
CHAPTER 6 PACKET 24	12
CHAPTER 6 PACKETS 27 / 0	13
not used	14
not used	15
PACKETS 8 / 30 / 0,1	16
PACKETS 8 / 30 / 2,3	17
PACKETS 8 / 30 / 4 to 15	18
not used	19 to 24

MBD788

Fig.10 Organization of the extension memory in enhanced mode.

VPT data memory organization

To simplify the software for dual-standard VPT decoders, the VPS data from line 16 is stored in row 25 of Chapter 5 of the page memory, and is aligned to match the packet 8/30 format 2 data as far as possible. The 8/30 format 2 packet is Hamming coded and by setting the appropriate register control bit the data is stored after hardware Hamming correction. There are 4 data bits stored in each column address of memory with an additional Hamming error bit. The data equivalent to the VPS signal is found in columns 12 to 19.

Although the VPS data is not Hamming protected, it is stored with 4 data bits per column address in the same way with an additional biphase error bit. The extra space in Row 25 is allocated to two more Line 16 words. They are Word 15 (reserved) and Word 4 (Program Source Identification, ASCII sequential) which may be useful for future applications. Details of the memory organization are shown in Fig.11.

The stored data can be read from memory via the I^{2}C-bus in the normal way. Multiple reception/majority error correction of the VPS data is the responsibility of the control software, the device simply stores the data as transmitted after biphase decoding.

As both VPS and 8/30/2 signals are stored in separate memory locations, it is possible to deal with future situations where both System A and System B transmissions may be present on the same TV channel, the defaults and level of service chosen by the control software.

column	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
8/30/2	D	initial page						b13	b14	b15	b16	b17	b18	b19	b20	b21	b22	b23	b24	b25
VPS	received page information										B11		B12		B13		B14		B15	

column	20	21	22	23	24	25	26	27	28	29	30	11	12	13	14	15	16	17	18	19
8/30/2	status display																			
VPS	B4		B5																	

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Fig.11 Detailed memory organization.

Register maps

IVT1.8* mode registers R0 to R13 are shown in Table 7. R0 to R10, R12 and R13 are WRITE only; R11 is READ/WRITE, R11B is read only. Register map (R3), for page requests, is shown in detail in Table 11.

Table 7 Register map (notes 1 to 4).

REGISTER NAME	No.	D7	D6	D5	D4	D3	D2	D1	D0
Advanced control	0	X/24 POS	FREE RUN PLL	AUTO $\overline{\text{ODD}}$/EVEN	DISABLE HDR ROLL	CBB SLAVE SYNC	DISABLE $\overline{\text{ODD}}$/EVEN	VCR MODE	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	$\overline{\text{7 + P}}$/ 8-BIT	ACQ $\overline{\text{ON}}$/OFF	EXT PKT ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	HAM CHECK 27, 8/30	BANK SELECT A2	ACQ CCT A1	ACQ CCT A0	0	SC2	SC1	SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	4	–	–	–	–	FREEZE HEADER ONLY	A2	A1	A0
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS $\overline{\text{BTM}}$/TOP	CURSOR ON	$\overline{\text{CONCEAL}}$/ REVEAL ON	$\overline{\text{TOP}}$/BTM HALF	$\overline{\text{SINGLE}}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1 to 23	BOX ON 0
Active chapter	8	–	–	–	VPS ENABLE	CLEAR MEM	A2	A1	A0
Cursor row	9	–	–	–	R4	R3	R2	R1	R0
Cursor column	10	–	–	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{\text{625}}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY
Advanced control 2A	12	H3	H2	H1	H0	S3	S2	S1	S0
Advanced control 2B	13	ENHANC MODE	CURSOR FREEZE/ DEVICE IDENT	MESHING ENABLE	VPS ENABLE	POINTS ENABLE	HAM CHECK 24 : 18	DISABLE PKT X/26	AUTO DISPLAY PKT X/24

Notes to Table 7

1. The dash (–) indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. Certain registers are auto-incremented following an I^2C-bus transmission byte. These are Register R0 to R3, R4 to R7 and R8 to R12 or R13.
3. All bits in Registers R0 to R13 are cleared to logic 0 on power-up except bits D0 and D1 of Registers R1, R5 and R6 which are set to logic 1.
4. All memory is cleared to space (00100000) on power-up, except Row 0 Column 7 Chapter 0, which is alpha white (00000111) as the acquisition circuit is enabled but all pages are on hold.

Table 8 Register description**.**

REGISTER BIT D0 TO D7	FUNCTION
R0 AVANCED CONTROL - auto-increments to Register 1	
$\overline{\text{R11}}$/R11B SELECT	Selects reading of R11 if LOW or R11B if HIGH.
VCR MODE	If logic 1 selects short time constant mode of PLL.
DISABLE $\overline{\text{ODD}}$/EVEN	Forces $\overline{\text{ODD}}$/EVEN output LOW when logic 1 (see Table 9).
CBB SLAVE SYNC	When set will modify internal slave sync timing to allow connection to sandcastle of Philips one-chip TV IC (TDA8362).
DISABLE HDR ROLL	Stops the display update of rolling time and green rolling header during page requests when logic 1. Time updates on page reception only.
AUTO $\overline{\text{ODD}}$/EVEN	If logic 1 then $\overline{\text{ODD}}$/EVEN output only active when no TV picture displayed (see Table 9).
FREE RUN PLL	Will force the display PLL to free run at 6 MHz when logic 1.
X/24 POS	Automatic display of FASTEXT prompt row when logic 1. Will also cause Row 24 data transmitted by packet 26 to be written to display, rather than extension memory.
R1 MODE - auto-increments to Register 2	
T0, T1	Interlace/non-interlace 312/313 line control (see Table 10).
TCS ON	Text composite sync or direct sync select (see Table 10 for FFB mode selection).
$\overline{\text{DEW}}$/FULL FIELD	Field-flyback or full-channel mode.
EXT PKT ENABLE	Enables reception and storage of extension packets when logic 1.
ACQ $\overline{\text{ON}}$/OFF	Acquisition circuits turned off when logic 1.
$\overline{\text{7 + P}}$/8-BIT	7 bits with parity checking or 8-bit mode.
VCS TO SCS	Connects VCS from video sync separater to display field sync detector to enable stable display of 60 Hz status messages when logic 1.
R2 PAGE REQUEST ADDRESS - auto-increments to Register 3	
SC0 to SC2	Start column for page request data (see Table 11).
0	Must be logic 0 for normal operation.
ACQ CCT A0, A1	Selects one of four acquisition circuits.
BANK SELECT A2	Selects bank of four pages being addressed for acquisition.
HAM CHECK 27, 8/30	8/4 Hamming check packet 27 and 8/30 data.
R3 PAGE REQUEST DATA - does not auto-increment	
PRD0 to PRD4	See Table 11.

REGISTER BIT D0 TO D7	FUNCTION
R4 DISPLAY CHAPTER - auto-increments to Register 5	
A0 to A2	Selects one of 8 display chapters.
FREEZE HEADER ONLY	Freezes the rolling header, but (unlike R0D4) allows the time to roll.
R5 NORMAL DISPLAY CONTROL - auto-increments to Register 6	
R6 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto-increments to Register 7; note 1	
PON	Picture on.
TEXT	Text on.
COR	Contrast reduction on.
BKGND	Background colour on.
R7 DISPLAY MODE - does not auto-increment	
BOX ON 0	Boxing function allowed on Row 0.
BOX ON 1 to 23	Boxing function allowed on Rows1 to 23.
BOX ON 24	Boxing function allowed on Row 24.
$\overline{\text{SINGLE}}$/DOUBLE HEIGHT	To display double height text.
$\overline{\text{TOP}}$/BTM HALF	To select bottom half of page when DOUBLE HEIGHT is logic 1.
$\overline{\text{CONCEAL}}$/REVEAL ON	To reveal concealed text.
CURSOR ON	To display cursor.
STATUS $\overline{\text{BTM}}$/TOP	Row 25 displayed above or below the main text.
R8 ACTIVE CHAPTER - auto-increments to Register 9	
A0 to A2	Active chapter for data written to or read from memory via the I^{2}C-bus.
CLEAR MEM	When set to logic 1, clears the display memory. This bit is automatically reset.
VPS ENABLE	VPS acquisition enabled when logic 1.
R9 CURSOR ROW - auto-increments to Register 10	
R0 to R4	Active row for data written to or read from memory via the I^{2}C-bus.
R10 CURSOR COLUMN - auto-increments to Register 11 or 11B	
C0 to C5	Active column for data written to or read from memory via the I^{2}C-bus.
R11 CURSOR DATA - does not auto-increment	
D0 to D7	Data read from/written to memory via I^{2}C-bus, at location pointed to by R9 and R10. This location automatically increments each time R11 is accessed.
R11B DEVICE STATUS - does not auto-increment	
VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase-locked to input video when logic 1.
TEXT SIGNAL QUALITY	If a good teletext signal is being received then logic 1.
ROM VER R0 to R4	Indicated language/ROM variant. For Western European is logic 0. R3 and R4 are set HIGH if R13 D6 is logic 1.
$\overline{\text{625}}$/525 SYNC	If the input video is a 525 line signal then logic 1.
R12 ADVANCED CONTROL 2A - does not auto-increment	
S0 to S3, H0 to H3	Each acquisition channel can be programmed to process its page in one of four ways as shown in Table 12.

REGISTER BIT D0 TO D7	FUNCTION
R13 ADVANCED CONTROL 2B - does not auto-increment	
AUTO DISPLAY PKT X/24	Status row will show the contents of the row of the extension memory (packet 24) when logic 1.
DISABLE PKT X/26	Output taken from processing engine written to the display memory when logic 0. Operates independent of the acquisition.
HAM CHECK 24 : 18	When logic 1 all packet 26 data is stored in extension memory unchecked.
POINTS ENABLE	Enable for acquisition pointers when logic 1.
VPS ENABLE	VPS acquisition enabled when logic 1.
MESHING ENABLE	Enables meshing display function in box mode.
CURSOR FREEZE/ DEVICE IDENT	When logic 1, cursor position not updated even if active row and column change. This bit will also cause R3 and R4 of the ROM code in Register R11B to be set HIGH. This allows software to identify the device as an IVT1.8*. An internal ‘1.8 mode’ flag is also set, which enables the operation of R0D4, R4D4 and the subtitle bit in R3.
ENHANC MODE	When logic 1, extension packet data is mapped into the last chapter. Only packet 24, 27/0 and 8/30 are stored. Chapters 0 to 6 can then be used for page storage. If extension packets are not enabled, 8 pages are stored as normal, but X/26 engine is enabled.

Note

1. These functions have IN and OUT referring to inside and outside the boxing function respectively.

Table 9 $\overline{\text{ODD}}$/EVEN selection.

AUTO $\overline{\text{ODD}}$/EVEN	DISABLE $\overline{\text{ODD}}$/EVEN	RESULT
0	0	$\overline{\text{ODD}}$/EVEN output continuous
0	1	$\overline{\text{ODD}}$/EVEN statically LOW
1	1	$\overline{\text{ODD}}$/EVEN active only when no TV picture displayed
1	1	$\overline{\text{DV}}$ output to indicate reception of error-free 8/30/format 2 packet or VPS line

Table 10 Interlace/non-interlace 312/313 line control and $\overline{\text{ODD}}$/EVEN field detection option.

TCS ON FFB MODE(2)	T1	T0	RESULT
X	0	0	interlaced 312.5/312.5 lines
X	0	1	non-interlaced 312/313 lines (note 1)
X	1	0	non-interlaced 312/313 lines (note 1)
0	1	1	SCS (scan composite sync) mode: FFB leading edge in first broad pulse of field
1	1	1	SCS (scan composite sync) mode: FFB leading edge in second broad pulse of field

Notes

1. Reverts to interlaced mode if a newsflash or subtitle is being displayed.
2. X = don't care.

Table 11 Register map for page requests (R3); notes 1 to 6.

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	DO CARE Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	DO CARE Page tens	PT3	PT2	PT1	PT0
2	DO CARE Page units	PU3	PU2	PU1	PU0
3	DO CARE Hours tens	SUBTITLE	X	HT1	HT0
4	DO CARE Hours units	HU3	HU2	HU1	HU0
5	DO CARE Minutes tens	X	MT2	MT1	MT0
6	DO CARE Minutes units	MU3	MU2	MU1	MU0
7	X	X	CH2	CH1	CH0

Notes

1. Abbreviations are as given in Table 6 except for DO CARE bits and CH = chapter address for acquisition chapter.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, normal or timed page selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I^2C-bus transmission bytes.
5. The SUBTITLE bit is only present when the device is in “1.8 mode” (i.e. R13D6 has been set HIGH).
6. X = don't care.

Table 12 Acquisition channel programming.

H0 to H3(1)	S0 to S3(1)	CHECKING ALGORITHM FOR ACQUISITION CHANNEL X
0	0	7-bit + parity for whole page
0	1	8-bit for whole page
1	0	8/4 Hamming check for whole page
1	1	mixed 8/4 Hamming (columns 0 to 7, 20 to 27) and 7-bit + parity (columns 8 to 19, 28 to 39)

Note

1. These register bits operate in conjunction with $\overline{7 + \text{P}}$/ 8-BIT (Register 1, Bit D6) which will over-ride the choice of data checker if set, setting all channels to 8-bit only. If this bit is not set H0 to H3 and S0 to S3 will determine the data checking (default to 7-bit + parity).

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional Colpitts 3-pin design operating at 27 MHz. The oscillator is sinusoidal and linear, with a controlled output amplitude. This reduces the radiated and conducted level of the 27 MHz fundamental frequency, and reduces the power dissipation in the quartz crystal. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.12. The crystal characteristics are given in Table 13.

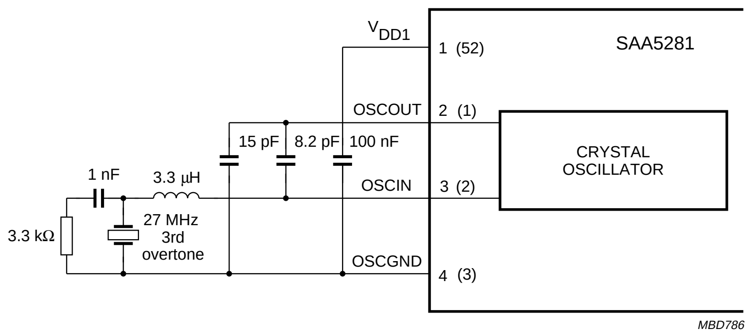


Fig.12 Crystal oscillator application diagram for SOT240-1; pins in parenthesis are for SOT247-1.

Table 13 Crystal characteristics (see Fig.12).

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)				
C1	series capacitance	1.7	–	pF
C0	parallel capacitance	5.2	–	pF
C_L	load capacitance	20	–	pF
R_r	resonance resistance	–	50	Ω
R1	series resistance	20	–	Ω
X_a	ageing	–	$\pm5 \times 10^{-6}$	$year^{-1}$
X_j	adjustment tolerance	–	$\pm25 \times 10^{-6}$	
X_d	drift	–	$\pm25 \times 10^{-6}$	

CHARACTER SETS

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in the Tables 18, 19 and 20 with reference to their table position in the basic character matrix illustrated in Table 17. The IVT1.8* automatically decodes transmission bits C12 to C14. Tables 14, 15 and 16 illustrate the character matrixes.

Character bytes are listed as transmitted from b1 to b7.

Meshing

This is an alternative method of displaying teletext subtitles, or similar boxed text superimposed on the TV picture and operates by showing reduced contrast TV pictures in place of the (black) background within the boxed area. The Meshing effect is produced by toggling the BLAN signal from IVT at pixel rate. By starting at the same point each field, and toggling the start position each line, a chequered pattern will result. This allows movement to be seen behind the text information. The MESH $\overline{\text{OFF}}$/ON bit in Register 13 D5 controls this function. Normally at zero, compatibility with IVT1.0 is maintained.

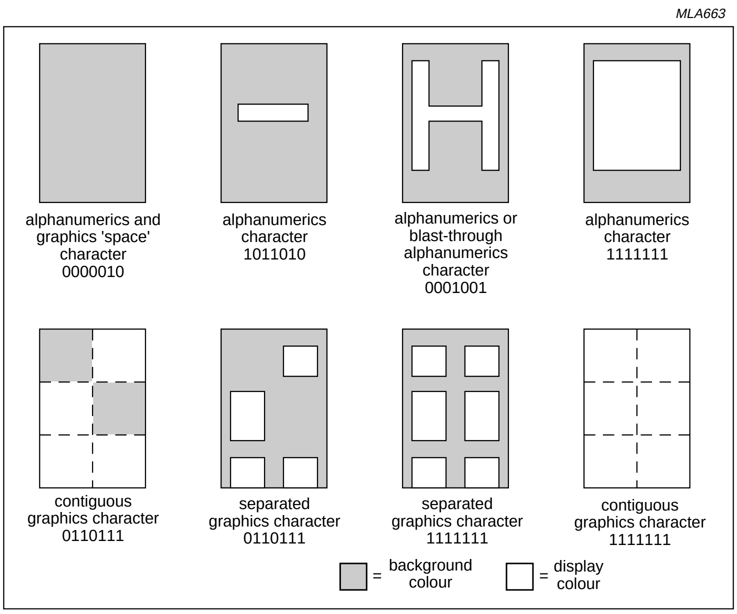


Fig.13 Character format.

Table 14 SAA5281P/E character data input decoding, West European languages; notes 1 to 9.

For character version number (11000) see Register 11B.

BITS b_4	b_3	b_2	b_1	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
				b_8	0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
				b_7	0	0	0	0	0	0	1	1	1		1		0	0	1	1	1	1
				b_6	0	0	1	1	1	1	0	0	1		1		0	0	0	0	1	1
				b_5	0	1	0	1	1	1	0	1	0		1		0	1	0	1	0	1
0	0	0	0	0	alpha - numerics black	graphics black			0		§	P	°		p		@	É	é	à	i	Á
0	0	0	1	1	alpha - numerics red	graphics red	!		1		A	Q	a		q		―	é	ù	è	¿	À
0	0	1	0	2	alpha - numerics green	graphics green	"		2		B	R	b		r		¼	ä	à	â	ü	È
0	0	1	1	3	alpha - numerics yellow	graphics yellow	#		3		C	S	c		s		£	#	£	é	ç	Í
0	1	0	0	4	alpha - numerics blue	graphics blue	$		4		D	T	d		t		$	¤	$	ï	$	Ï
0	1	0	1	5	alpha - numerics magenta	graphics magenta	%		5		E	U	e		u				ã	Ã	ª	Ó
0	1	1	0	6	alpha - numerics cyan	graphics cyan	&		6		F	V	f		v				õ	Õ	º	Ò
0	1	1	1	7	alpha - numerics white (2)	graphics white	'		7		G	W	g		w				•	Ç	Ñ	Ú
1	0	0	0	8	flash	conceal display	(		8		H	X	h		x		‖	ö	ò	ô	ñ	æ
1	0	0	1	9	steady (2)	contiguous graphics (2)	)		9		I	Y	i		y		¾	å	è	û	è	Æ
1	0	1	0	10	end box (2)	separated graphics	*		:		J	Z	j		z		÷	ü	ì	ç	à	ð
1	0	1	1	11	start box	ESC (1)	+		;		K	Ä	k		ä		←	Ä	°	ë	á	Đ
1	1	0	0	12	normal height (2)	black back - ground (2)	,		<		L	Ö	l		ö		½	Ö	ç	ê	é	ø
1	1	0	1	13	double height	new back - ground	–		=		M	Ü	m		ü		→	Å	→	ù	í	Ø
1	1	1	0	14	SO (1)	hold graphics	.		>		N	^	n		β		↑	Ü	↑	î	ó	þ
1	1	1	1	15	SI (1)	release graphics (2)	/		?		O	_	o		■		#	_	#	#	ú	Þ

MBA429

Table 15 SAA5281P/H character data input decoding, East European languages; notes 1 to 9.
For character version number (11001) see Register 11B.

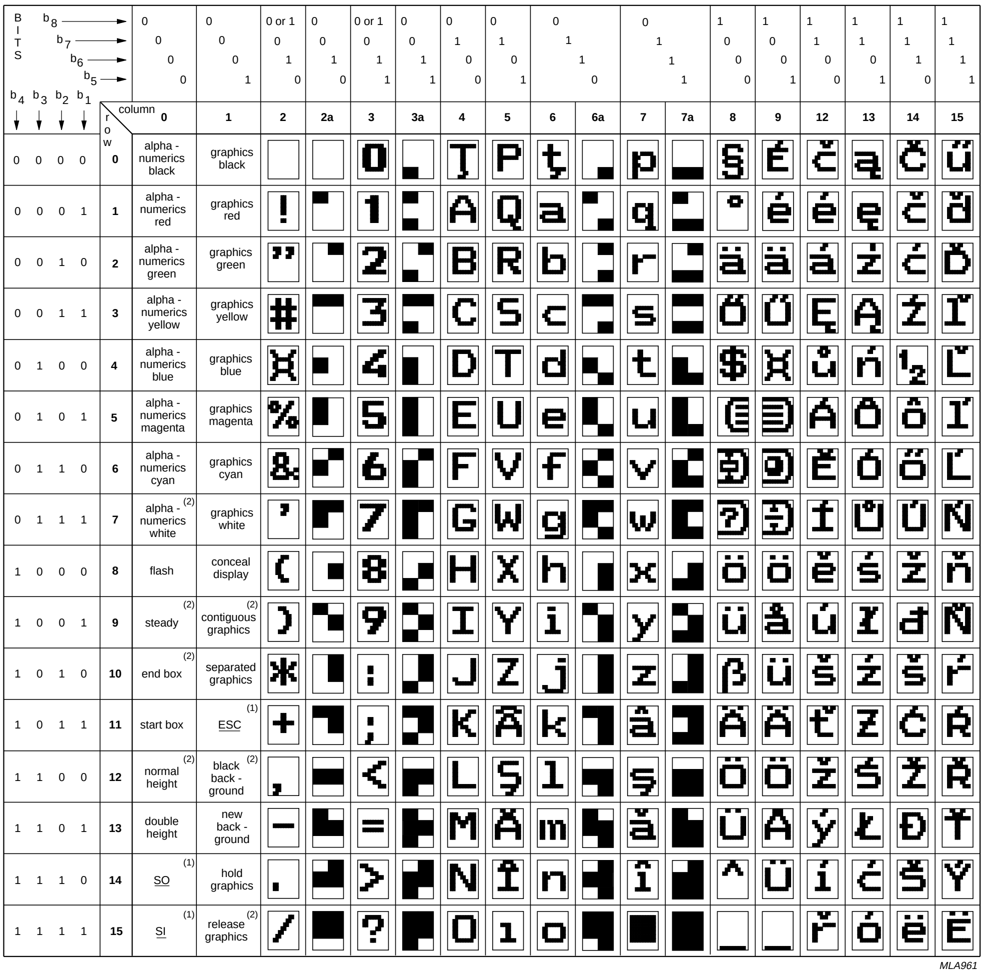
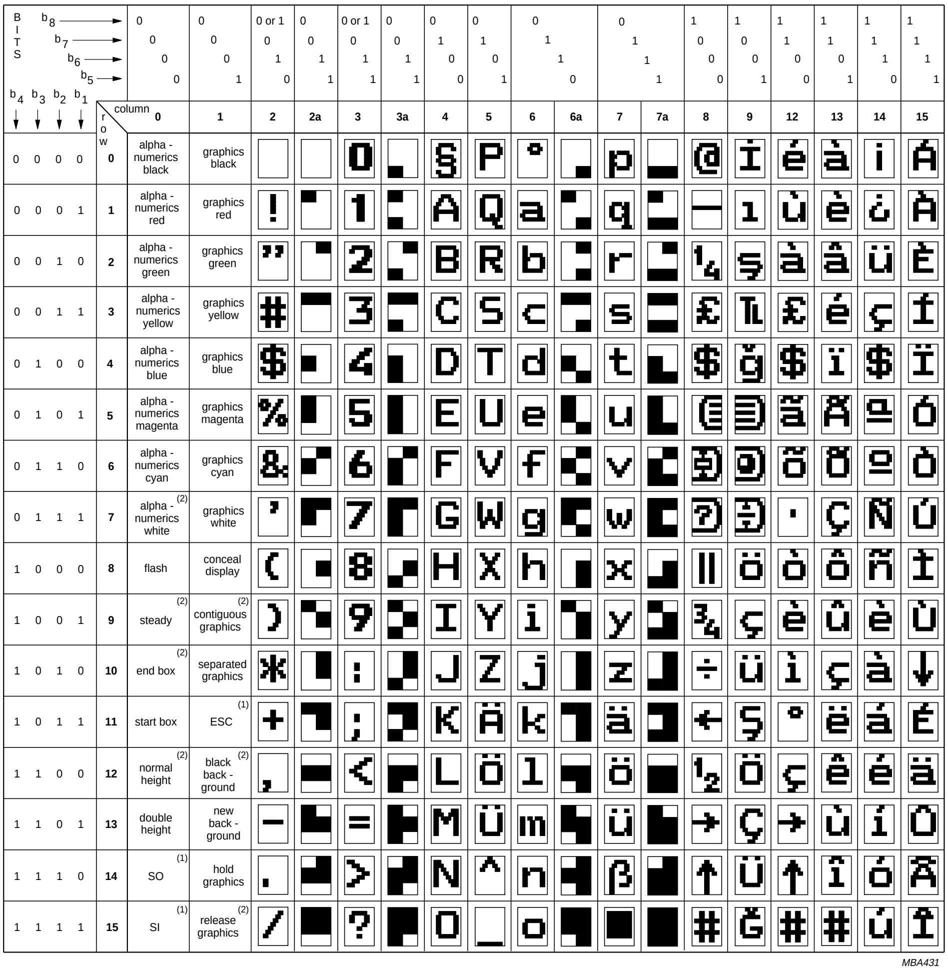


Table 16 SAA5281P/T character data input decoding, West European and Turkish languages; notes 1 to 9.

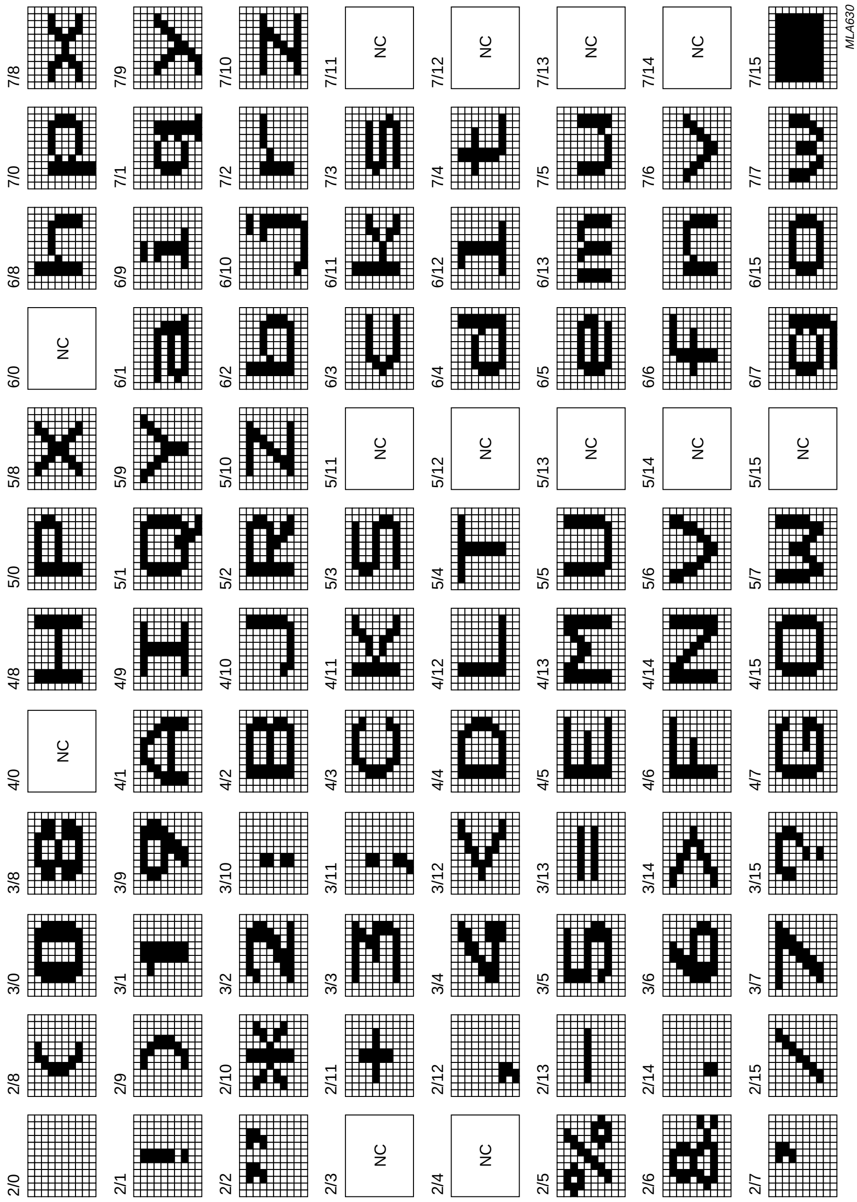
For character version number (11010) see Register 11B.



Notes to Tables 14, 15 and 16

1. These control characters are reserved for compatibility with other data codes.
2. These control characters are presumed before each row begins.
3. Control characters shown in Columns 0 and 1 are normally displayed as spaces.
4. Characters may be referred to by column and row (for example 2/5 refers to %).
5. Black represents displayed colour. White represents background.
6. The SAA5281 national option characters are illustrated in Tables 18, 19 and 20.
7. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5 (E, H and T codes only). Characters 5/12, 5/13, 5/14 and 5/15 are combined with 5/11 (S code only).
8. National option characters will be displayed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Tables 18, 19 and 20.
9. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 17 SAA5281 basic character matrix; note 1.



Note

1. Where NC = national option character position.

Table 18 SAA5281P/E national option character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MLB458

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Table 19 SAA5281P/H national option character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
POLISH	0	0	0	#	ń	ą	Ƶ	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAKIA	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

MLA966

(1) PHCB are the Page Header Control Bits. Other combinations default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 17.

Table 20 SAA5281P/T national option character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	**2 / 3**	**2 / 4**	**4 / 0**	**5 / 11**	**5 / 12**	**5 / 13**	**5 / 14**	**5 / 15**	**6 / 0**	**7 / 11**	**7 / 12**	**7 / 13**	**7 / 14**
ENGLISH	**0**	**0**	**0**	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	**0**	**0**	**1**	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
TURKISH	**1**	**1**	**0**	TL	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ITALIAN	**0**	**1**	**1**	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	**1**	**0**	**0**	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	**1**	**0**	**1**	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MBA430

(1) PHCB are the Page Header Control Bits. Other combinations default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 17.

APPLICATION INFORMATION

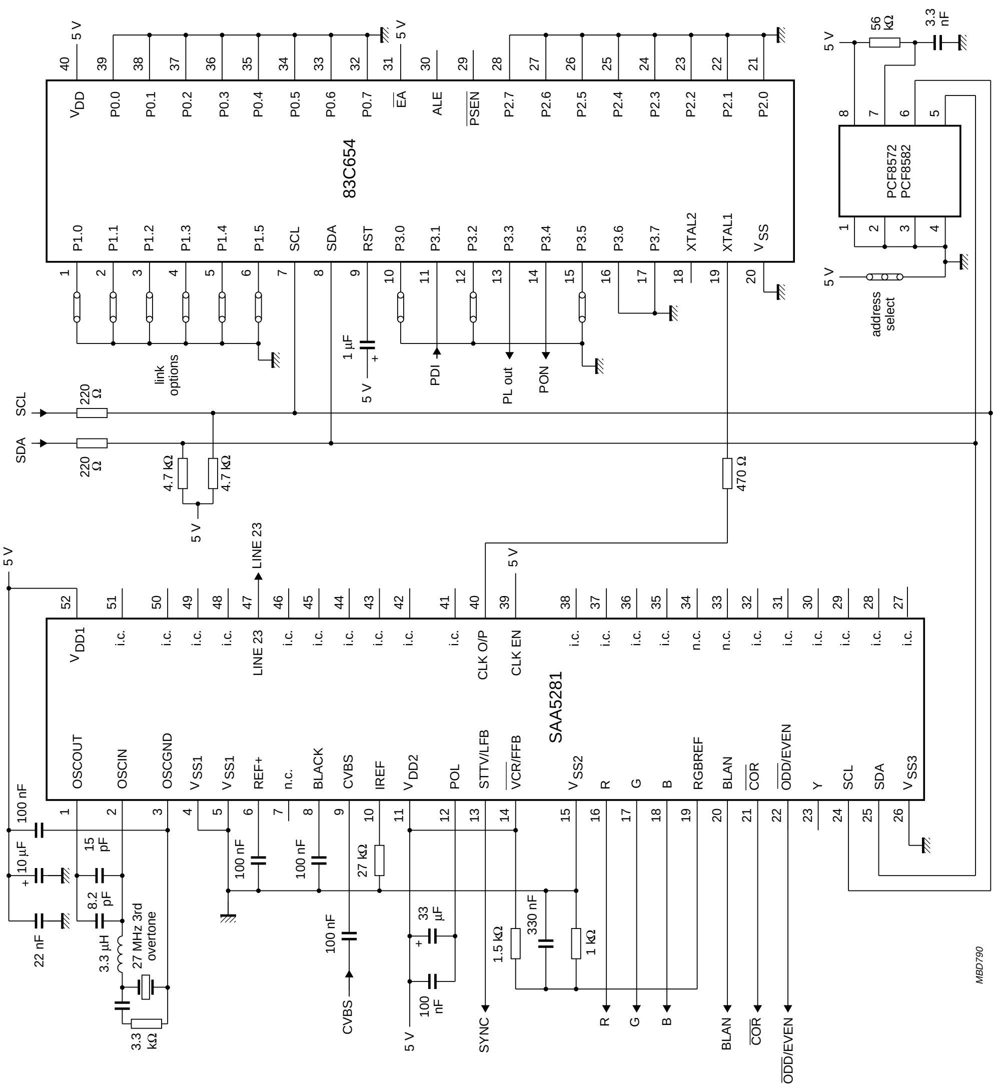
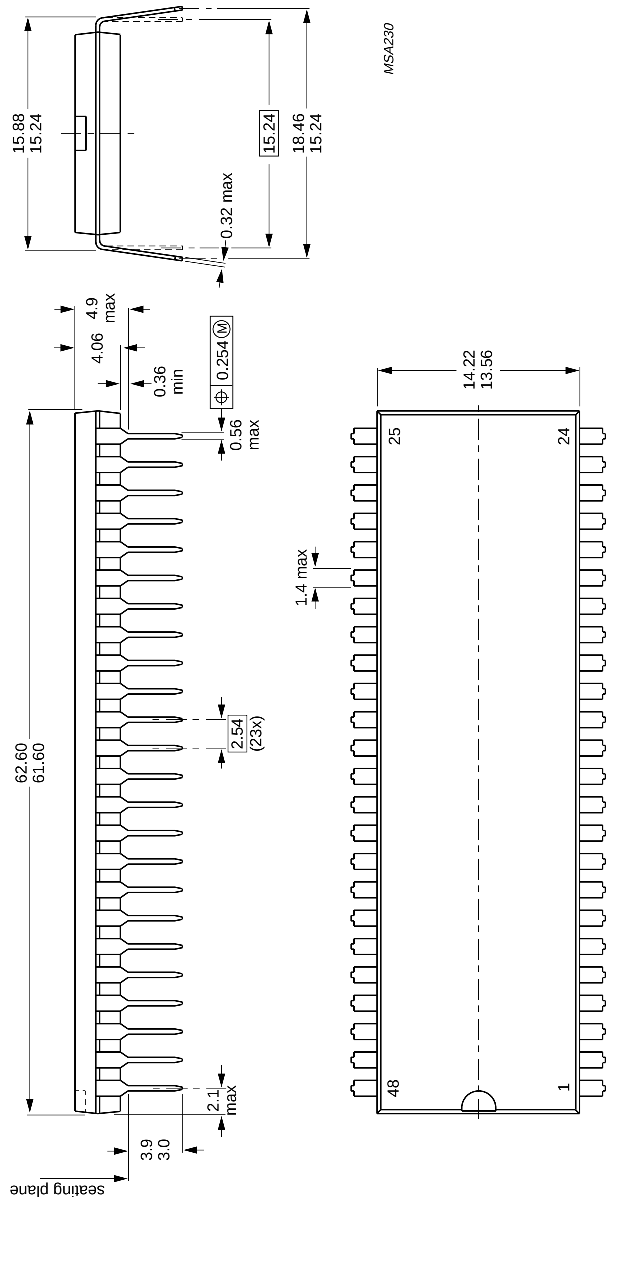


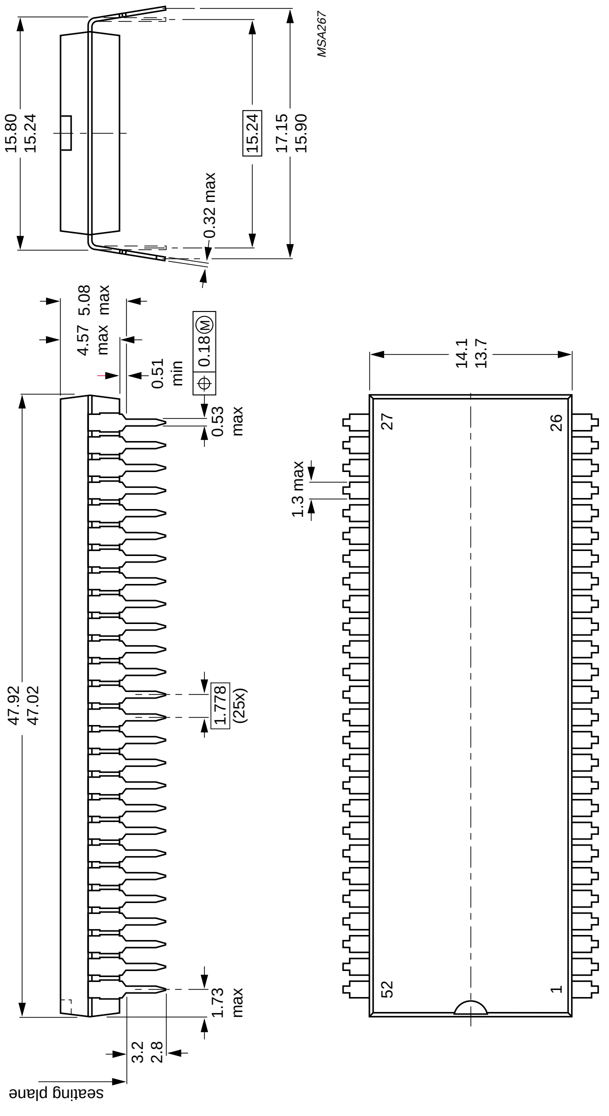
Fig.14 Application diagram for SDIP52, SOT247-1.

PACKAGE OUTLINES



Dimensions in mm.

Fig.15 Plastic dual in-line package; 48 leads (600 mil); DIP48, SOT240-1.



Dimensions in mm.

Fig.16 Plastic shrink dual in-line package; 52 leads (600 mil); SDIP52, SOT247-1.

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, foJune 1994rced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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